Reg. No. | | | | | | | | | | |

Sixth Semester B.E. Degree Examination, August 200

Electronics & Communications

VHDL

17

[Max.Marks : 100

me: 3 hrs.]

Note: *Answer any FIVE full questions.*
All questions carry equal marks.

1. (a) Give a comparison between the symbol and entity with an example (6 Marks)

   (b) Explain the following statements
   i) Process ii) Architecture iii) Configuration iv) Concurrent (2×4=8 Marks)

   (c) Write the behavioral descriptem for EXOR and EXNOR gates (3×2=6 Marks)

2. (a) Explain the significance of Block statments in VHDL. Give an example using the guarded block statements. (10 Marks)

   (b) Develop a VHDL code for a Buffer using Trnasport delay model and Inertial delay model. (5 Marks)

   (c) Write a VHDL code for implementing on S-R FF (5 Marks)

3. (a) Bring out the differences between signal alignment and variable alignment (4 Marks)

   (b) Using basic gates develop a VHDL code for a full adder (6 Marks)

   (c) Explain any FIVE types of sequential statements along with BNF and an example for each (10 Marks)

4. (a) Develop a VHDL code for a 4:1 multiplexer using PROCESS statement (8 Marks)

   (b) Write a function for implementing a T flip-flop and use it in configuring a three bit counter. (12 Marks)

5. (a) Explain the different types of functions with suitable examples (12 Marks)

   (b) Write a behavioral description for a BCD ripple counter (8 Marks)

6. (a) Explain the different types of configuration statements with an example (12 Marks)

   (b) Develop VHDL code for a three bit shift register the have right shift and left shift operations. (8 Marks)

7. (a) Explain the following w.r.t. Syntheris (i) RTL (ii) Constraints (12 Marks)

(b) Write the RTL description that uses component instantiation for D flip flop. (8 Marks)

8. Write short notes on

(a) Drivers

(b) File types

(c) Packages

(d) Procedures (20 Marks)

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EC/TE6108

Reg. No.

Sixth Semester B.E. Degree Examination, February 2002

Electronics and Communication/Telecommunications Engineering

VHDL

18

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*
All questions carry equal marks.

1. (a) Explain the following with an example for each
   i) Component instantiation
   ii) Event scheduling
   iii) Concurrent signal assignment. (3 × 3=9 Marks)

   (b) Write a VHDL program for the function
   $y = AB + C\overline{D}$ using
   i) Behavioural description
   ii) Structural description. (5+6=11 Marks)

2. (a) Explain the simulation deltas with the help of a buffer circuit. (8 Marks)

   (b) Write a VHDL program for a 4 bit decade counter using J/K flip flops. (6 Marks)

   (c) Using Guarded block statements write a VHDL program for a D latch. (6 Marks)

3. (a) With a BNF and an example for each explain
   i) IF statement
   ii) LOOP statement
   iii) ASSERT statement
   iv) WAIT statement. (4 × 3=12 Marks)

   (b) Explain the significance of PROCESS statement with an example of a 4bit full adder. (8 Marks)

4. (a) Name the different scalar data types and explain each with an example. (10 Marks)

   (b) Distinguish between single dimensional array and multi dimensional array with an example of 8 bit comparator and a 16 × 16 pixel array. (10 Marks)

5. (a) With the following illustration explain the function and procedure : generate
   $f_1 = \overline{a}b + bc\overline{d} + abcd$
   $f_2 = \overline{c}d + a\overline{b}$ (6 Marks)

   (b) Write a VHDL program to convert a model from designer A to designer B such that

$$'X' - 'X'; 'L' - 'O'; 'H' - 'I'; 'Z' - 'Z'$$

(5 Marks)

6. (a) Bring out the differences between lower level configuration and ENTITY - ARCHITECTURE pair configuration. (8 Marks)

(b) Explain the importance of Board - Socket - chip analogy. (4 Marks)

(c) Using the Board - Socket - chip analogy write a VHDL program for D flip flops. (8 Marks)

7. (a) Explain the register transfer level description with an example. (10 Marks)

(b) Write a VHDL program for a 4 bit shifter using sequential statements. (10 Marks)

8. Explain

a) Statement Concurrency

b) Block statement

c) Sub program

d) Synthesis

(4 × 5=20 Marks)

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EC/TE6D1

Reg. No.

Sixth Semester B.E. Degree Examination, July/August 2002

Electronics and Communication/Telecommunications Engineering

VHDL

19

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Explain briefly the terms:

   i) Architecture ii) Configuration

   iii) Generic iv) Process (4×2=8 Marks)

   (b) Give the structural and behavioural description of SR flip flop. (6+6=12 Marks)

2. (a) Explain concept of concurrent statements and event scheduling with examples. (8 Marks)

   (b) Explain port delay, inertial delay and simulation delta in VHDL. (12 Marks)

3. (a) Explain following sequential statements if, case, loop, assert and wait with examples. (10 Marks)

   (b) Write a VHDL program to select the largest of 3 integers. (10 Marks)

4. (a) Explain the various data types of VHDL with examples. (12 Marks)

   (b) Write a VHDL program for a 8 to 3 encoder operation. (8 Marks)

5. (a) Bring out the differences between single dimension and multi dimension arrays with examples. (8 Marks)

   (b) Write a VHDL program for a mux when input 'a' is selected the process waits for changes on 'select' and 'a' and ignores changes on 'b'. Similarly if 'b' is selected changes in 'a' is to be ignored. (12 Marks)

6. (a) Explain record types and incomplete types. (6 Marks)

   (b) Write a VHDL program to simulate the operation of a stack for read/write purposes. (14 Marks)

7. (a) Explain lower level configuration with examples and entity architecture configuration with examples. (8 Marks)

   (b) Using configuration statement realise a full adder circuit using two half adders and a or gate. Write the VHDL program both for full adder and half adder and bind them using configurations. (12 Marks)

8. (a) Describe the file types and packages. (10 Marks)

   (b) Explain RTL descriptions and block statements with examples. (10 Marks)

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Reg. No. | | | | | | | | | | |

LIBRARY EC/TE601

Sixth Semester B.E. Degree Examination, January/February 2003

Electronics and Communication/Telecommunications Engineering

VHDL

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Explain the following VHDL terms with an example for each.
   i) Entity ii) Process
   iii) Attribute iv) Generic (8 Marks)
   (b) Write a program for 1 bit full adder with a) Behavioral b) Structural c) Sequential description. (4 × 3=12 Marks)

2. (a) Describe briefly event scheduling, statement concurrency and simulation data, with example. (9 Marks)
   (b) Compare transport and inertial delay. (3 Marks)
   (c) With example explain block and guarded block statements. (8 Marks)

3. (a) List i) Concurrent statements ii) Sequential statements (4 Marks)
   (b) Explain the following statement
   a) with select b) case c) loop d) assert (8 Marks)
   (c) Write a VHDL code for JK flip flop with clear and set inputs. (8 Marks)

4. (a) List various data types used in VHDL. Explain any 4 types with example. (10 Marks)
   (b) Compare procedures and functions. (4 Marks)
   (c) Write a function to convert a binary number to integer. (6 Marks)

5. (a) Explain package and package body. (8 Marks)
   (b) Write a conversion function in package and use that in a program. (8 Marks)
   (c) Define deferred constant. Write an example for deferred constant. (4 Marks)

6. (a) Describe briefly configuration. Show the difference between default and component configuration with an example: (8 Marks)
   (b) Write a note on block configuration. (4 Marks)
   (c) Write a VHDL code for synchronous 8 bit updown counter with asynchronous clear input. (8 Marks)

7. (a) Explain briefly RTL description (5 Marks)

   (b) Write a note on state machine in VHDL code. (5 Marks)

   (c) Write a VHDL code for 8 bit universal shift register with serial, parallel data input and left and right shift. (5 Marks)

8. Write short notes on any FOUR :

   (a) Component instantiation

   (b) Test bench

   (c) Subprograms

   (d) Constraints

   (e) Attributes

(4 x 5=20 Marks)

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USN | | | | | | | | | | |

Sixth Semester B.E. Degree Examination, July/August 2003

Electronics & Communication / Telecommunication Engineering

VHDL

21

Time: 3 hrs.] [Max.Marks : 100

Note: 1. *Answer any FIVE full questions.*
2. *All questions carry equal marks.*

1. (a) Explain the following with example
   i) Entity ii) Architecture
   iii) Statement concurrency iv) Driver (12 Marks)

   (b) Differentiate behavioral & structural programming, by considering a common example of half-subtractor. (8 Marks)

2. (a) What is generic? Explain with an example of entity AND-gate having 3 generics associated with it, rise time, fall time & load and a model that instantiates the components of type AND. (7 Marks)

   (b) Explain with an example (8 Marks)
   i) Inertial delay ii) Transport delay.

   (c) Why are block statements are essential in modelling? Explain with example. (5 Marks)

3. (a) Write the structure of process statement? Explain each part. (8 Marks)

   (b) Explain WAIT statement in its different forms, with examples. (6 Marks)

   (c) Write the behavioral code for D flip flop with asynchronous reset and preset. (6 Marks)

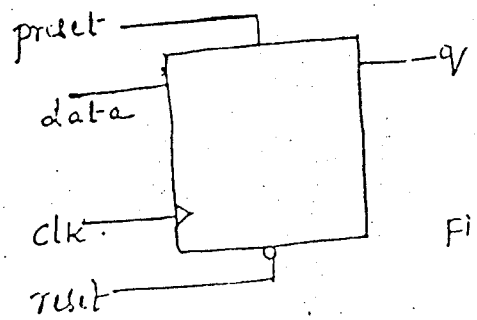

Fig 3(c)

4. (a) Compare signal assignment and variable assignment with example. (4 Marks)

   (b) List the data types in VHDL. Explain any two types with example, showing type declaration and object declaration of that type. (8 Marks)

Contd.... 2

(c) Write the behavioral code to simulate 5 byte ROM. The ROM is provided with active-low chip select line & an address line. (8 Marks)

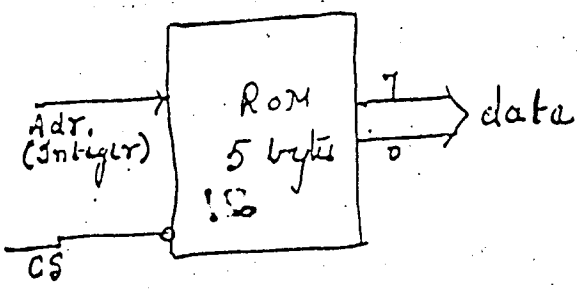

Fig 4(c)

5. (a) Explain procedure and function with syntax and a common example of finding the average of two numbers. (10 Marks)

(b) Write the package structure and explain its parts, with an example. (6 Marks)

(c) What is deferred constant? Give an example. (4 Marks)

6. (a) Explain configuration. Compare default configuration & component configuration. (8 Marks)

(b) Write VHDL code to simulate 4 - bit a - synchronous counter (up). The code should have JK flip-flop (behavioral) program and counter (structural) program. Use configurations, to bind them. (12 Marks)

7. (a) Explain RTL description with example. (10 Marks)

(b) Explain the following with respect to synthesis:
i) constraint ii) attribute iii) technology library. (10 Marks)

8. Write short notes on:
i) Library in VHDL
ii) Composite data type
iii) Event scheduling.
iv) ASSERT Statement. (4×5=20 Marks)

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USN

Sixth Semester B.E. Degree Examination, January/February 2004

Electronics & Communication / Telecommunication Engineering

VHDL

22

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Write a VHDL program to simulate 4 : 1 MUX functionality using conditional assignment statement. (8 Marks)

   (b) Explain briefly the statement concurrency with the help of a simple VHDL program. (7 Marks)

   (c) Differentiate inertial delay and transport delay with the help of timing diagrams. (5 Marks)

2. (a) Write a VHDL program to model N-input NAND gate. Use generics and exit statement. (6 Marks)

   (b) Differentiate signal assignment and variable assignment, with an example. (4 Marks)

   (c) Write a VHDL program to model shift register with shift right PIPO and restore status facilities. Use generate statement. (10 Marks)

3. (a) Explain with an example vector the following operations. (6 Marks)

   i) sll ii) sra iii) ror.

   (b) Write a simple VHDL program to demonstrate shift left and right operations using concatenation operator. (7 Marks)

   (c) Write a function subprogram to model 4 : 1 MUX circuit. (7 Marks)

4. (a) Write a 3-8 decoder model using VHDL. use file 1 to store and assign signal values for all input ports and use another file to store output of decoder. (10 Marks)

   (b) Write a procedure subprogram to model demux circuit. (10 Marks)

5. (a) Write a package and package body to include few type declarations, constants a procedure and a function. (12 Marks)

   (b) Write ALU model (for add, sub, rot, shift right, NOT, XOR, AND and OR operations) using case statement. Use enumerated data type. (8 Marks)

6. (a) Write state diagram and its implementation in VHDL for "101" sequence detector. (10 Marks)

   (b) Write RTL description for MOD-9 counter and the coresponding VHDL program. (10 Marks)

Contd.... 2

7. (a) Explain the following in the Leonarado synthesis environment

i) RTL level description ii) Constraints iii) Attributes

iv) Technology libraries. (3×4 Marks)

(b) Write VHDL model for the following schematic shown in fig.7(b). Use block configuration

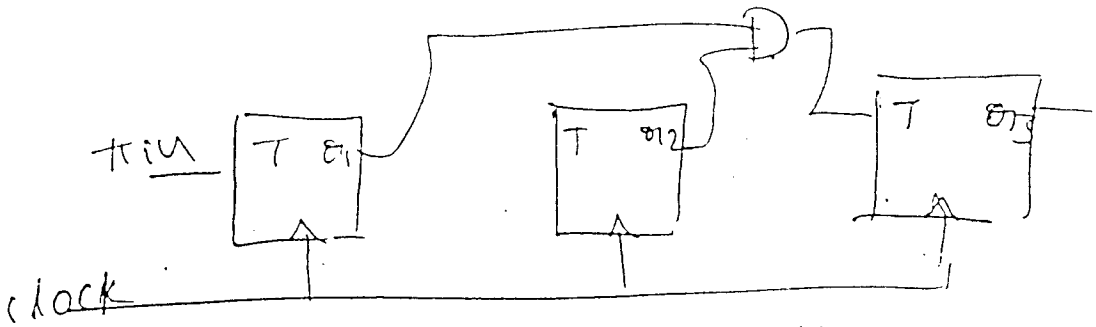

Fig 7(b)

(8 Marks)

8. Write short notes on : (4×5 Marks)

i) CAD tools for VLSI design

ii) Justify the use of VHDL for design entry

iii) Circuit synthesis

iv) Physical data types

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EC/TE6D1

USN

Sixth Semester B.E. Degree Examination, July/August 2004

Electronics & Communication/Telecommunication Engineering

VHDL

Time: 3 hrs.] [Max.Marks : 100

Note: *1. Answer any FIVE full questions.*
2. All questions carry equal marks.

1. (a) Describe the following with suitable example.

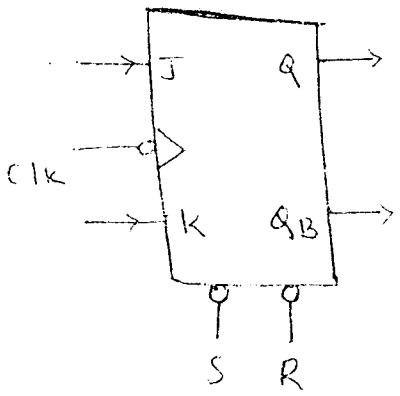
i) Symbols V/s Entities (4 Marks)

ii) Schematic V/s Architecture (4 Marks)

iii) Event scheduling. (2 Marks)

(b) What are the advantages of VHDL over traditional design, explain. (4 Marks)

(c) Write the VHDL behaviour description for the JK flip-flop shown (fig.1(c)) and explain. (6 Marks)



← fig 1(c)

2. (a) Explain delta delay mechanism and any other delay mechanism with suitable example. Compare the two mechanisms. (10 Marks)

(b) Explain the syntax of "WITH SELECT" statement with an example. (6 Marks)

(c) Write VHDL program for D latch using guarded block statement. (4 Marks)

3. (a) Explain with example "Sensitivity list versus WAIT statement". (6 Marks)

(b) Explain the BNF of "ASSERT Statement" with suitable example. (8 Marks)

(c) Write VHDL code for structural description of 4-bit adder. (6 Marks)

4. (a) Write behaviour code for four bit shift register with parallel load and serial output and explain. (8 Marks)

(b) Explain with an example each :

i) Enumerated data type ii) Physical data type. (6 Marks)

(c) Explain VHDL objects with suitable example. (6 Marks)

Contd.... 2

5. (a) Explain 'function' with syntax and write VHDL code for converting array of std-logic type to integer using 'function'. (10 Marks)

   (b) What is resolution function? Explain with VHDL code the resolution function for 4 value system. (10 Marks)

6. (a) Discuss with suitable example architecture that contains instantiated components can be configured. (10 Marks)

   (b) What is default configuration? Explain with example how default configuration can be used to bind architecture to an entity. (10 Marks)

7. (a) Write VHDL model using two process style to describe the 4 bit counter with clear and load. (7 Marks)

   (b) Explain synthesis process. (5 Marks)

   (c) Define Mealy machine and Moore machine. Describe Moore machine with an example. (8 Marks)

8. Write short note on :

   a) Access type data
   b) Procedure
   c) Attributes
   d) Generics.

(4×5=20 Marks)

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EC/TE6D1

USN

Sixth Semester B.E. Degree Examination, January/February 2005

Electronics & Communication / Telecommunication Engineering

VHDL

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Explain the following with a suitable example for each :
   i) Event scheduling
   ii) Concurrent signal assignment/ statement concurrency
   iii) Guarded block statement. (4×3=12 Marks)

   (b) Explain the concept of behavioral description and structural description using half-adder as an example. (8 Marks)

2. (a) Describe the concept of inertial delay and transport delay. Develop a VHDL code for a buffer using inertial delay model and transport delay model. (10 Marks)

   (b) Write VHDL coding for a T flip-flop using PROCESS with a sensitivity list. Include an assertion statement in your model, which expresses the requirement that a flip-flop's two outputs Q and Qb of the type Std-logic are complementary. (10 Marks)

3. (a) Write a VHDL behavioral model of a 4-bit counter with asynchronous reset and preset facilities. (10 Marks)

   (b) Explain the following sequential statements along with BNF and give an example for each:
   i) CASE ii) WAIT (6 Marks)

   (c) Bring out the differences between signal assignment and variable assignment. (4 Marks)

4. (a) Explain the following data types with suitable example:
   i) Enumerated type ii) Physical type (6 Marks)

   (b) Indicate the significance of ARRAY type declaration. Write VHDL code for modelling a ROM of capacity 8×4 bits. (10 Marks)

   (c) Write a RECORD type of declaration for a test stimulus record containing a stimulus bit vector of 3-bits, a delay value and an expected response bit vector of 8-bits. (4 Marks)

5. (a) Bring out the differences between functions and procedures. Give the general format for subprogram declaration and the corresponding calling statement. (8 Marks)

Contd.... 2

(b) Write a complete VHDL code to perform the following operation : use a function to convert the input array to integer, determining the maximum of three numbers in integer and outputting the value in array using functions and packages. (12 Marks)

6. (a) Define the resolution function. Discuss in detail the resolution function for a four value system. (10 Marks)

(b) Explain the different types of configuration statements with suitable examples. (10 Marks)

7. (a) Explain the following with respect to synthesis i) RTL ii) Constraints (10 Marks)

(b) Explain the various steps involved in the conversion of RTL description to gate level net list. (10 Marks)

8. (a) Write a VHDL program for a 4-bit shifter using sequential statements. The shifter is to be provided with a facility of loading and shifting to right or left by one bit at a time. (10 Marks)

(b) Discuss in brief :

i) Package declaration and package body (6 Marks)

ii) Generics. (4 Marks)

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NEW SCHEME

EC64

Reg. No.

Sixth Semester B.E. Degree Examination, January/February 2006
Electronics & Communication/Telecommunication Engineering
Digital System Design Using VHDL

Time: 3 hrs.) (Max.Marks : 100

Note: *Answer any FIVE full questions.*

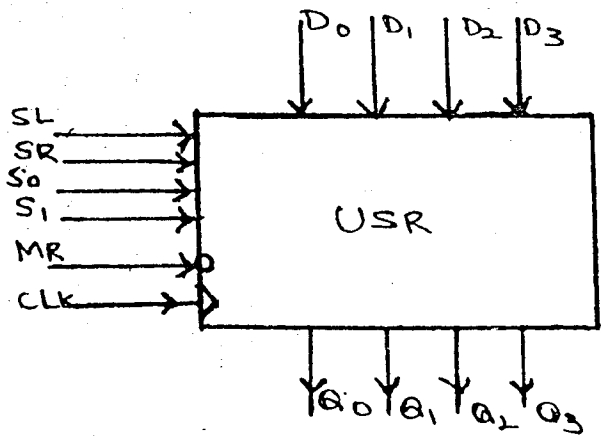
1. (a) Explain briefly :
   i) Entity architecture pair
   ii) Package in VHDL. **(5+5 Marks)**

   (b) Write a VHDL code for a full subtracter using logic equation. **(6 Marks)**

   (c) If A=1100, B=1110, C=1001, compute Y_1 = not A and B nor 2
   Y_2 = B sla 2 and C sll 2. **(4 Marks)**

2. (a) What is meant by variables, signals and constants in VHDL? Compare signals with variables, give an example for each. **(10 Marks)**

   (b) Write a VHDL module for a universal shift register with following functions. MR Active low, a synchronous reset I/P that resets all flipflops. Two control inputs $(S_1 S_0)$ when 00, no action, when 10, register is shifted right and serial data SR enters Q_0, when 01, 4 bit data shifted left and SL enters Q_3. If $S_1 S_0 = 11$, 4 bit data is loaded parallely. **(8 Marks)**



   (c) Specify the general form of case statement. **(2 Marks)**

3. (a) Realize the following functions using PLA.

$$F_1 = \sum m(2,3,5,7,8,9,10,11,13,15)$$

$$F_2 = \sum m(2,3,5,6,7,10,11,14,15)$$

$$F_3 = \sum m(6,7,8,9,13,14,15)$$

   Write VHDL code for implementation of F_1, F_2 *and* F_3. **(6+6 Marks)**

Contd.... 2

(b) Write a VHDL code for D flipflop that reports error for setup and hold time violation. Assume set up time = hold time = 5ns and display text string as violation of setup Or hold time. (8 Marks)

4. (a) Write state diagram that generates control signals for 4x4 bit multiplier. Explain with block diagram. (8 Marks)

(b) Design signed multiplier and write a VHDL code to multiply two signed numbers. (6+6 Marks)

5. (a) Derive a SM chart to realize DICE game. (10 Marks)

(b) Using PLA and D flip flops realize the SM chart for the dice game. (10 Marks)

6. (a) Explain briefly with neat sketch Kilink 3000 series I/O block. (8 Marks)

(b) Write a function Fadd Ion VHDL to realize full adder operation. Design 4 bit parallel adder using full adders and write behavioral model for 4 bit parallel adder that uses function Fadd. (6+6 Marks)

7. (a) What is meant by attributes. Explain signal attribution with an example for each. (2+6 Marks)

(b) Write a VHDL code for T flipflop. Using T flipflop as component write structural model for 8 bit up counter. Assume active low asynchronous clear input and falling edge triggered clock.
Use Generate statement (2+4 Marks)

(c) Write a VHDL module for memory model (RAM6116). Assume 8 bit address lines, 8 bit data lines, active low chip enable and active low write enable. (6 Marks)

8. Write short notes on any FOUR :

(a) Transport and inertial delay

(b) Generic

(c) Signal resolution

(d) Modeling mealy machine

(e) VHDL procedures. (5 x 4=20 Marks)

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EC 64

USN

NEW SCHEME

Sixth Semester B.E. Degree Examination, July 2006
E & C
Digital System Design using VHDL

Time: 3 hrs.] [Max. Marks:100

Note: Answer any FIVE full questions.

1 a. Explain structural and behavioral description with examples. **(08 Marks)**

b. Differentiate between : i) Signal and variable assignment
ii) Event and transactions. **(06 Marks)**

c. Write a VHDL program for detecting the number of 1's in an eight bit-vector. If even, it should output 'O'; if odd, output = '1'. **(06 Marks)**

2 a. If A = 110101 B = 110010 , compute (A S112) OR (B S1A3) **(04 Marks)**

b. A Moore sequential machine with two inputs x1 and x2 and output z has the following state table.

State	X1 X2				Z
	0 0	0 1	1 0	1 1	
1	1	1	2	2	0
2	1	2	2	1	1

Write the VHDL code at behavioral level. State changes occur after 5 ns and output changes occur 5 ns after state changes. **(08 Marks)**

c. Realize using ROM and DFF and write the VHDL code using ROM table for

PS	NS		
	W = 0	W = 1	Z
0 0	0 0	0 1	0
0 1	0 0	1 0	0
1 0	1 0	0 1	0
1 1	1 0	0 1	1

(08 Marks)

3 a. Find a minimum row PLA table to implement the following sets of functions

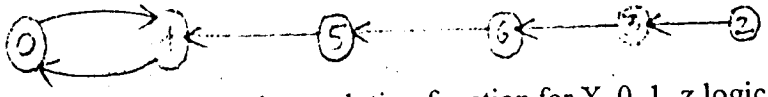
f_1 (A,B,C,D) = $\sum$ m (3,4,6,9,11)

f_2 (A,B,C,D) = $\sum$ m (2,4,8,10,11,12)

f_3 (A,B,C,D) = $\sum$ m (3,6,7,10,11)

and realize these functions using a PLA. **(06 Marks)**

b. A counter has the count sequence as shown. Realise the counter using 16 R4 PAL. Draw the section of the PAL where this function is implemented.



(10 Marks)

c. Write a VHDL code for the resolution function for X, 0, 1, z logic. **(04 Marks)**

Contd...2

4 a. Draw and explain the block diagram of a [illegible] converter and write the state graph for the same. (08 Marks)

b. Draw the block diagram, state graph and VHDL program for the behavioral model of a 4 x 4 multiplier. (12 Marks)

5 a. Design and explain an 8 bit divider wherein dividend is 8 bit and divisor [illegible] shift and subtract action should take place in the same cycle. Draw the [illegible] diagram and state diagram. (10 Marks)

b. Give the contents of the dividend register with respect to clock cycle for the dividend and divisor. Shift and subtract in separate clock cycles.

Dividend – 0 1 1 1 0 0 0 0 1 0 divisor [illegible] (10 Marks)

6 a. For the following Sm chart give the timing diagram showing the clock, states [illegible] and output. Give the PLA table.

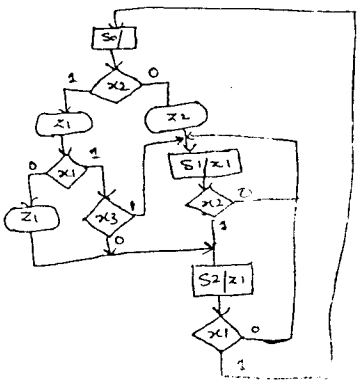


Fig. 6 (a) (10 Marks)

b. Implement a bit binary counter using one Xilinx 3000 series logic cell. Qx is the LSB bit and Qy is the MSB of the counter. The counter has an [illegible] and a synchronous load. The counter operates as follows :

En = 0	no change
En = 1 . Ld = 1	load Qx and Qy with inputs u and v
En = 1 Ld = 0	2 increment count

i) Give the next state equations for Qx and Qy

ii) Label the inputs on the FG mode diagram and show the connection paths. (10 Marks)

7 a. Write a VHDL code for a static Ram with truth table (08 Marks)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	mode	I/o pins
H	X	X	not selected	high z
L	H	H	output disabled	high z
L	L	H	read	data out
L	X	L	write	Data in

b. Write a VHDL function that will find the dot product $\sum ai * bi$ of two integer vectors a and b. (06 Marks)

c. Explain signal attributes with examples. (06 Marks)

8 a. Explain the Xilinx 3000 series logic cell (07 Marks)

b. Explain transport and inertial delays with examples. (06 Marks)

c. Write a VHDL code and synthesized circuit for case statement. (07 Marks)

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EC64

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NEW SCHEME

Sixth Semester B.E. Degree Examination, Dec. 06 / Jan. 07
EC / TE
Digital System Design Using VHDL

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Using a single bit subtractor, write a VHDL code for 4-bit subtractor. **(08 Marks)**

b. Differenciate between the conditional assignment statement and single assignment statement with respect to 4 : 1 Mux. **(06 Marks)**

c. What are the predefined unconstrained arrays? Explain each with an example. **(06 Marks)**

2 a. Bring out the differences between VHDL function and VHDL procedure with an example. **(06 Marks)**

b. Draw the structure of a 8-bit counter using 74163. Write a VHDL description for a 8-bit counter using 74163 model. **(08 Marks)**

c. Write a VHDL code for synthesis of a sequential CASE statement. **(06 Marks)**

3 a. Write a VHDL description that converts a 5-bit bit_vector to an integer. **(08 Marks)**

b. Realize the following functions using PLA : **(06 Marks)**

$f_1(a,b,c,d) = \sum m(2,3,5,7,8,9,10,11,13,15)$,

$f_2(a,b,c,d) = \sum m(2,3,5,6,7,10,11,14,15)$ and $f_3(a,b,c,d) = \sum m(6,7,8,9,13,14,15)$

c. Model the tristate buffers with active – high output enable. **(06 Marks)**

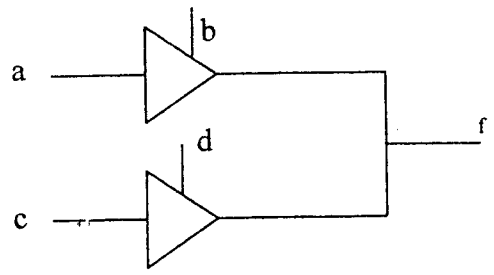
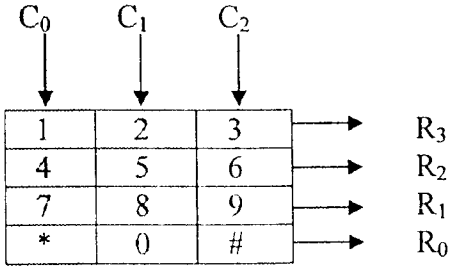


Fig.3(c)

4 a. Design a 6-bit binary up-down counter using a 22V10 and a minimum number of external gates. Write the VHDL code for the counter using PLA. **(10 Marks)**

b. Design a keypad scanner for the following keypad layout. **(10 Marks)**



Contd...2

5 a. Design a 4-bit serial adder with accumulator and generate the control state graph and table which defines the operation of a serial adder. **(08 Marks)**

b. Write a VHDL module that describes one bit of a full adder with accumulator . The control i/p Ad = 1 add operation and Load = 1 load the i/p to the accumulator. **(06 Marks)**

c. Write a VHDL code for 2 input Nor gate with Rise / Fall time modeling using generic statement. **(06 Marks)**

6 a. Write a test-bench for the Dice game problem to test the game components. **(10 Marks)**

b. The functional equivalent of a static RAM cell is as shown in figure. Write a VHDL code to realize the functionality **(10 Marks)**

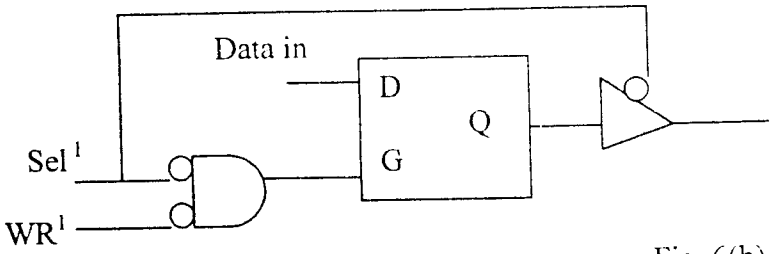


Fig. 6(b)

7 a. Give sequence of simulator commands that would test the divider for the case 93 divided by 17. **(06 Marks)**

b. Write a VHDKL code for the resolution function for X 0 1 Z logic. **(06 Marks)**

c. Realize the SM chart given using a PLA, counter and 4-1 Mux. **(08 Marks)**

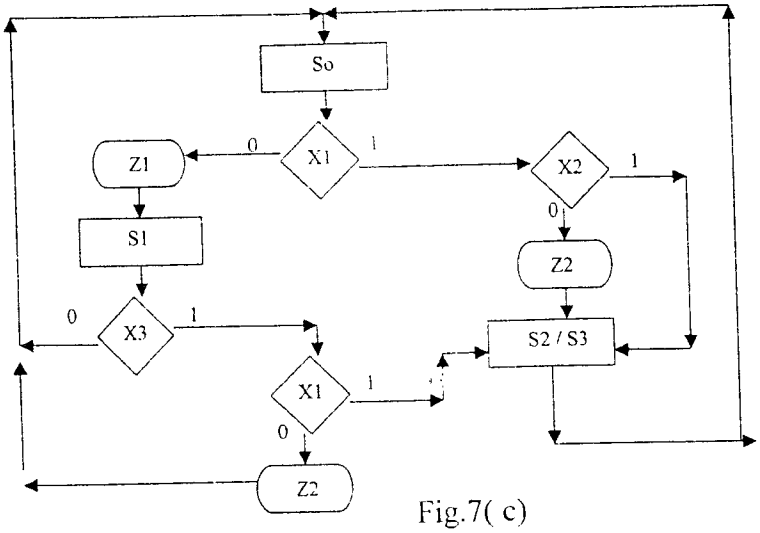


Fig.7(c)

8 a. Show how to realize the following combinational function using two 3000 series logic cells. **(10 Marks)**

$F = X_1^1 X_2 X_3^1 X_6 + X_2^1 X_3^1 X_4 X_6^1 + X_2 X_3^1 X_4^1 + X_2 X_6 X_4^1 X_6 + X_3^1 X_6 X_4 X_5 X_6^1 + X_7$

b. Write a VHDL code using One-hot assignment for the following specifications

To : Q0 Q1 Q2 Q3 = 1000 ; T1 = 0100 ; T2 = 0010 ; T4 = 0001

$Q3^+ = X1\ Q0 + X2\ Q1 + X3\ Q2 + X4\ Q3$; $Z1 = X1\ Q0 + X3\ Q2$;

$Z2 = X2\ Q1 + X4\ Q3$; **(10 Marks)**

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EC64

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NEW SCHEME

Sixth Semester B.E. Degree Examination, July 2007
EC / TE
Digital System Design Using VHDL

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Write down the VHDL-code to model the following :
   i) D-flip flop
   ii) J-K flip flop
   iii) 4 : 1 multiplexer **(09 Marks)**
   b. Starting from a single bit full adder as a component, write down the structural VHDL description for a 4 bit adder. **(06 Marks)**
   c. With the help of a block diagram, explain the stages of compilation, elaboration and simulation. **(05 Marks)**

2 a. Develop the VHDL code for 8 bit counting using IC 74163 binary synchronous counters. Show the hardware diagram. **(06 Marks)**
   b. Explain with a set of statements, the sequential execution using process and if else statements. Assume suitable delays wherever necessary. **(06 Marks)**
   c. Implement a Mealy sequential network with ROM and D-flip flops for BCD to excess 3 code convertor. Draw the ROM truth table and ROM realization code. **(08 Marks)**

3 a. Using CMOS-PLD 22CE V10, design a VHDL code for a sequential traffic light controller. Supply the necessary state graph and state table. **(10 Marks)**
   b. For a keypad scanner (4 rows × 3 columns), develop a VHDL code incorporating key bouncing. Supply the stategraph for scanner and truth table for decoder. **(10 Marks)**

4 a. Draw the state graph for binary multiplier control and hence develop a behavioral VHDL model for binary multiplier. **(10 Marks)**
   b. Draw the block diagram for a signed divider (32 bits by 16 bits) with the associated control circuits. Supply the steps of procedure to carry out the division. Draw the state graph for control circuit. **(10 Marks)**

5 a. Describe the design of a serial adder with accumulator supplying the block diagram control state graph and state table. **(10 Marks)**
   b. Derive an SM chart for the control of unsigned binary multiplier (4 bits × 4 bits). Convert this SM chart into VHDL code. **(10 Marks)**

Contd.... 2

6 a. For the dice game based on the following rules, draw the SM chart and develop the behavioral VHDL code.

i) After the first roll of the dice the player wins if the sum is 7 or 11. The player loses if the sum is 2, 3 or 12. Otherwise, the sum the player obtained on the first roll is referred to as a point and he or she must roll the dice again.

ii) On the second or subsequent roll of the dice, the player wins if the sum equals the point, and he or she loses if the sum is 7. Otherwise, the player must roll again until he or she finally wins or loses. **(10 Marks)**

b. With Xilinx XC 3020, implement a parallel adder-subtractor with an accumulator. Show a typical logic design cell with inputs and outputs, and signal paths shown after programming. **(10 Marks)**

7 a. Assuming that configuration data is available in EPROM, outline the steps of procedure to design any digital system using FPGA. Give one example of design. **(10 Marks)**

b. Explain IEEE-1164 standard logic system for use with VHDL taking one VHDL code example. **(10 Marks)**

8 a. Develop a VHDL code for a RAM system with data register, memory control and MAR, giving block diagram and the corresponding SM chart. **(10 Marks)**

b. Write the separate SM charts for simplified 486 bus interface with CPU and for UART receiver. **(10 Marks)**

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EC64

Sixth Semester B.E. Degree Examination, Dec. 07 / Jan. 08
Digital System Design Using VHDL

Time: 3 hrs. Max. Marks:100

Note : *Answer any FIVE full questions.*

1 a. Explain the following with declaration format and an example each:
i) Variable ii) Signal iii) Constant **(06 Marks)**

b. Using a process statement write a VHDL source code for 4 to 1 multiplexer. **(06 Marks)**

c. Bring out differences between a VHDL function and a VHDL procedure with a suitable example. **(08 Marks)**

2 a. The data stored in the ROM location are (9, A, 0, 0, 1, 0, 0, 1, F, C, C, D, 7, 4, 6, 7). Write a VHDL code for the ROM realization by using the binary values of the numbers given above. **(06 Marks)**

b. Find a minimum row PLA table to implement the following set of functions.

$f_1(A,B,C,D) = \sum m(3,4,6,9,11)$

$f_2(A,B,C,D) = \sum m(2,4,8,10,11,12)$

$f_3(A,B,C,D) = \sum m(3,6,7,10,11)$ **(09 Marks)**

c. A keypad has 4 rows and 3 columns as shown in figure Q2 (c)

1	2	3
4	5	6
7	8	9
*	0	#

Fig. Q2 (c)

Assume no more than two keys will be pressed at a time. Write the block diagram of keypad scanner and first 10 rows of the truth table for a keypad decoder. If 2 keys are pressed in the same column, the N output should indicate the key in the first of the 2 rows. **(05 Marks)**

3 a. With a neat block diagram and the function tables, explain the operation of a serial adder with accumulator. **(06 Marks)**

b. The state graph for faster multiplex (4 × 4) is as shown in figure Q3 (b). Write a behavioral model (VHDL source code) for 2's complement 4 × 4 binary multiplier. **(07 Marks)**

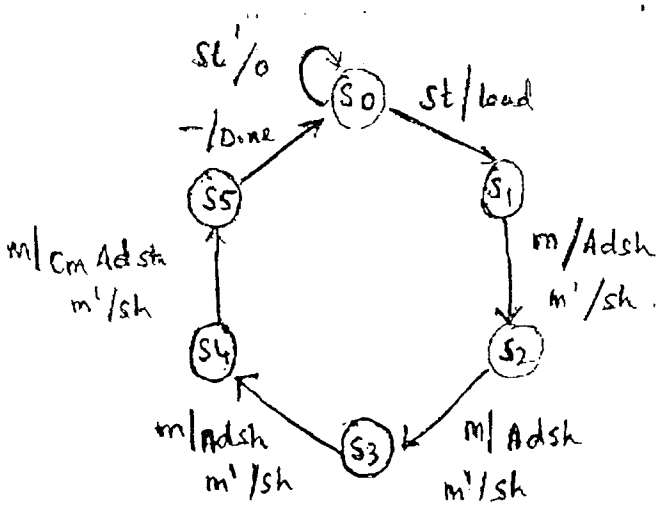

Fig. Q3 (b)

3 c. Design a binary divider and draw the block diagram of the same. Show the procedure to divide 135 by 13 [convert it into binary and perform the operations]. (07 Marks)

4 a. Derive the state machine (SM) chart for dice game and obtain the state graph for dice game controller. (10 Marks)

b. Write a VHDL description of the state machine band on SM chart. (10 Marks)

Present state	Next state				Output z_1 z_2			
	$x_1 x_2$ =00	01	10	11	$x_1 x_2$ =00	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

5 a. Explain in brief with necessary SM charts, the linked state machines. (06 Marks)

b. Discuss the programmable interconnects between the CLB (Configurable Logic Blo and I/O blocks with respect to

i) General purpose interconnects. (08 Marks)

ii) Direct interconnects.

c. With a neat diagram explain the CLB as a Read / Write memory cell of Xilinx 4000 series FPGA. (06 Marks)

6 a. Design a floating point multiplier, explicitly showing the exponent adder, fraction multiplier and control network. (10 Marks)

b. Explain operator over loading and write a source code for VHDL package with overloaded operation for bit-vectors. (06 Marks)

c. Write a VHDL code for the following tristate buffers with active – high output enable (figure Q6 (c)). (04 Marks)

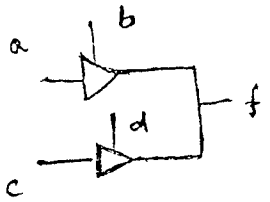

Fig. Q6 (c)

7 a. Write a VHDL source code to 4 bit adder using generate statement. (04 Marks

b. With a neat block diagram and truth table explain the 6116 static RAM. (07 Marks

c. Explain the simplified 486 bus model with a microprocessor bus interface and timin diagram of intel 486 basic 2 – 2 bus cycle. (09 Marks

8 Write short notes on:

a. Compilation / Simulation.

b. VHDL operators.

c. Synthesis.

d. Programmable Array Logic (PALs). (20 Mar

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